**Basic Electronics (ENG 111) Lab Manual**

**2nd Semester (2018-19)**

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**Department of Electronics and Communication Engineering**

**School of Engineering and Applied Sciences**

**SRM University-AP, Amaravati**

**List of Experiments**

1. Verification of Kirchhoff’s laws (KCL, KVL).
2. Study of I-V characteristics of PN junction diode.
3. Design of half-wave rectifier using PN junction diode with and without capacitor filter.
4. Design of positive and negative clipping circuits using PN junction diodes.
5. Study of current and voltage gain characteristics of a NPN transistor in common-emitter configuration.
6. Design of inverting and non-inverting amplifier circuits using op-amp IC 741.
7. Study of integrator and differentiator circuits using op-amp IC 741.
8. Design of an oscillator circuit using IC 555 timer.
9. Study of low-pass and high-pass filter circuits using RC components.
10. Study of function of digital logic gates (AND, NOT, OR, NAND, NOR).

**Experiment 1**

**Verification of Kirchhoff’s laws**

**Aim:** The aim of the experiment is to verify Kirchhoff’s current law (KCL) and Kirchhoff’s voltage law (KVL) in a given circuit.

**Apparatus:**

NI ELVIS II

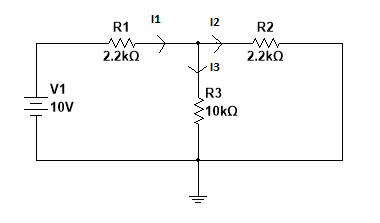
Connecting probes

Resistors (2.2 k, 2.2k, 10k)

Multisim (virtual digital multimeter)

Connecting wires

**Circuit diagram:**

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**Procedure:**

1. Connect the circuits diagram on the ELVIS II bread board using the components and connecting wires.
2. Measure the voltage across R1 (2.2 k) resistor using the connecting probes and virtual multimeter in Multisim.
3. The current passing through the resistor R1 is calculated using the Ohm’s law.
4. Similarly, the voltage across resistors R2 and R3 will calculated using the virtual multimeter and further currents.
5. KCL will be verified at Node N using the currents.
6. Similarly, KVL will be verified at loop 1 and loop 2 using the voltage drops.

**Results:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Resistor** | **Voltage** | **Current** |
| **1** | **R1** |  |  |
| **2** | **R2** |  |  |
| **3** | **R3** |  |  |

**Calculations: Using the measured voltage drops across the resistors,**

1. Verification of KCL at Node 1 is given below:
2. Verification of KVL in loop 1 and loop 2 is given below:

**Conclusions:**

**Experiment 2**

**Study of V-I Characteristics of PN Junction Diode**

**Aim:** To study the Volt-Ampere Characteristics of Silicon P-N Junction Diode in forward and reverse bias conditions.

**Apparatus:**

NI ELVIS II

Variable DC power supply

Resistors (1k)

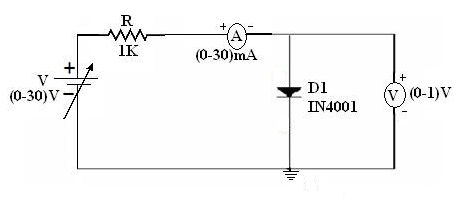
Diode (IN4001)

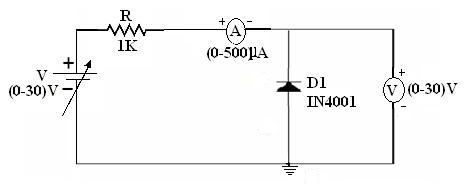
Multisim (virtual digital multimeter)

Connecting wires

**Circuit diagram:**

**Forward Bias:**

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**Reverse Bias**

**Procedure:**

**Forward Biased Condition:**

1. Connect the PN Junction diode in forward bias i.e. P-terminal is connected to positive of the power supply and N-terminal is connected to negative of the power supply.
2. Use a variable DC power supply and a series resistance of1kΏ.

The series resistance is used to limit the current flowing to the diode.

1. For various values of forward voltage (Vf) across the diode note down the corresponding values of forward current(If) flowing in the diode.
2. Increase the variable power supply in steps of 0.3 V until 2V and thereafter increase in steps of 1 V and tabulate Vf and If values. Use the variable power supply to its maximum value available in the ELVIS.

**Reverse biased condition:**

1. Connect the PN Junction diode in Reverse bias i.e., P-terminal is connected to negative of the power supply and N-terminal is connected to positive of the power supply.
2. Use a variable DC power supply and a series resistance of 1 kΩ.
3. For various values of (Vr) note down the corresponding values of reverse current (Ir).
4. Increase the variable supply voltage in steps of 1V and tabulate Vr and Ir values in the reverse bias condition.

**Results:**

**Forward Bias:**

|  |  |  |
| --- | --- | --- |
| **Variable DC supply (V)** | **Vf (volts)** | **If (mA)** |
| 0.3  0.6  0.9  1.2  1.5  1.8  2  4  6  8  10  12 |  |  |

**Reverse Bias:**

|  |  |  |
| --- | --- | --- |
| **Variable DC supply (V)** | **Vf (volts)** | **If (µA)** |
| 1  2  3  4  5  7  9  11  12 |  |  |

**Conclusions:**

**Experiment 3**

**Design of Half-Wave Rectifier using PN junction Diode**

**Aim**: To design half wave rectifier circuit to convert AC voltage to DC.

**Apparatus:**

NI ELVIS II

Virtual Function generator

Resistors (1k)

Diode (IN 4001)

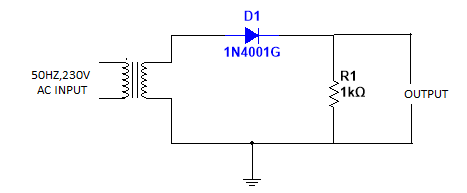
Multisim

Virtual oscilloscope

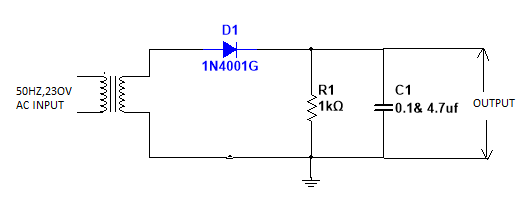
Connecting wires

**Circuit diagram:**

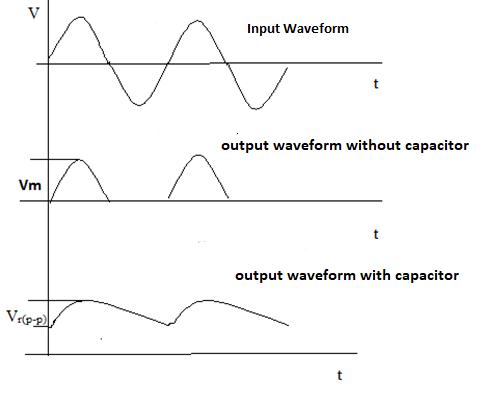
**Without Capacitor:**



**With Smoothing Capacitor**



**Expected Waveforms:**

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**Procedure:**

1. Give the connections as per the circuit diagram.
2. Apply 10 V peak to peak AC voltage from function generator across the load resistor.
3. Observe the o/p across the load resistor using the virtual CRO.
4. Repeat steps 2 and 3 by inserting a smoothing capacitor of value 47 µF parallel to the load as shown in the circuit and calculate the ripple voltage across the load resistor.
5. Repeat step 4 by inserting a smoothing capacitor of value 220 µF.
6. Calculate the ripple voltage across the capacitor using the formula given below.

**Calculations:**

Vr = Ripple voltage

Vp = Peak voltage of rectifier output

f = Frequency of input supply (50 Hz)

R = Load resistor

C = Smoothing capacitor

VD = Forward voltage drop across the diode (usually 0.6 V)

1. Calculate the DC voltage and ripple voltage for 47µF:
2. Calculate the DC voltage and ripple voltage for 220 µF:

**Conclusions:**

**Experiment 4**

**Design of Positive and Negative Clipping Circuits Using PN Junction Diode**

**Aim**: To design positive and negative clipping circuit using PN junction diode.

**Apparatus:**

NI ELVIS II

Virtual Function generator

Resistors (2.2k)

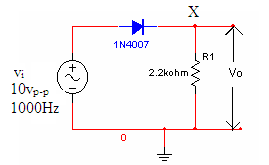
Diode (IN 4001)

Virtual oscilloscope

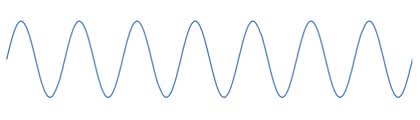
Connecting wires

**Circuit diagram:**

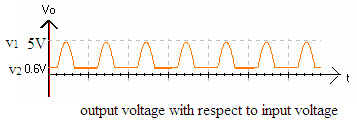
**Negative Clipper**

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**Input Signal**

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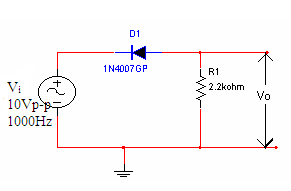
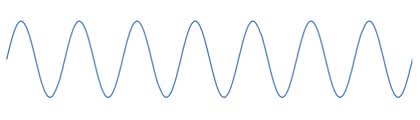
**Output Signal**

****

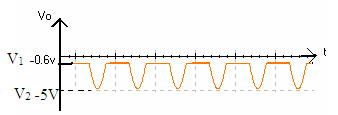
**Circuit diagram:**

**Positive Clipper**

**Input Signal**

 ****

**Output Signal**



**Procedure:**

1. Give the connections as per the circuit diagram.
2. Apply 10 V peak to peak AC voltage from function generator across the PN junction diode
3. Observe the output across the load resistor using the virtual CRO.
4. Measure peak-to-peak voltages of the output.

**Conclusions:**

**Experiment 5**

Study of current and voltage gain characteristics of a NPN transistor in common-emitter configuration.

Aim: To Study DC Current and Voltage gain for the Common Emitter Configuration.

**Apparatus:**

NI ELVIS II+

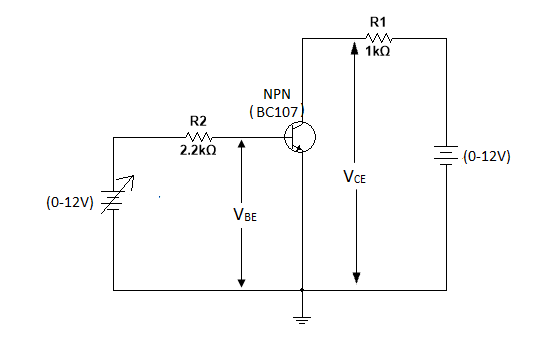
Resistors (2.2K, 1K)

Transistor (BC107)

Virtual DC Power Supply

Connecting wires

**CIRCUIT DIAGRAM**:

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Procedure:

1. Connect the circuit diagram on the NI ELVIS II+ bread board using the components and connecting wires.
2. Connect the 15 V fixed power supply across the collector-emitter terminals.
3. Connect the variable power supply across base-emitter terminals
4. Emitter terminal is connected to ground which is common for both input and output.
5. Vary the base-emitter voltage and note down the base current and collector current.

Calculations:

Output current, ; Input current,

**Observation Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S no | VBB(V) | IB (uA) | IB (mA) | β | AV |
| 01 | 0.3 |  |  |  |  |
| 02 | 0.7 |  |  |  |  |
| 03 | 1.0 |  |  |  |  |
| 04 | 1.5 |  |  |  |  |
| 05 | 2.0 |  |  |  |  |

Conclusions:

**Experiment 6**

**Design of Inverting and Non Inverting Amplifier Using 741 Operational Amplifier**

Aim: Design of Inverting and Non Inverting Amplifier Using 741 Op-amp.

**Apparatus:**

NI ELVIS II

Connecting probes

Resistors (100 k, 1k,)

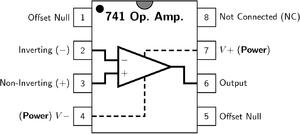
Multisim (virtual function generator, virtual CRO)

IC 741

Connecting wires.

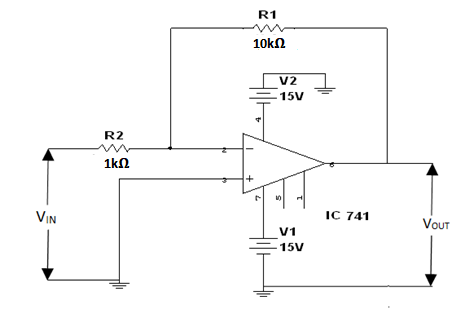
**Circuit diagram:**

**IC 741 PIN Diagram**

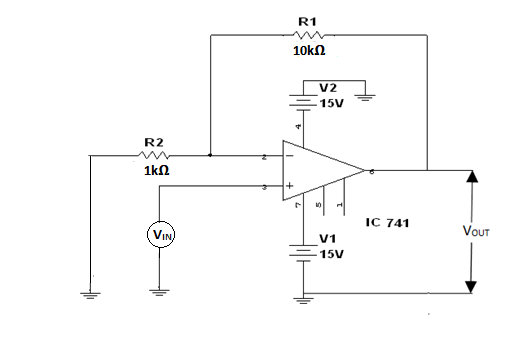




**INVERTING AMPLIFIER:**

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**NON- INVERTING AMPLIFIER:**

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**Procedure:**

1. Connect the circuit for inverting amplifier as given in the figure above on NI ELVIS board.

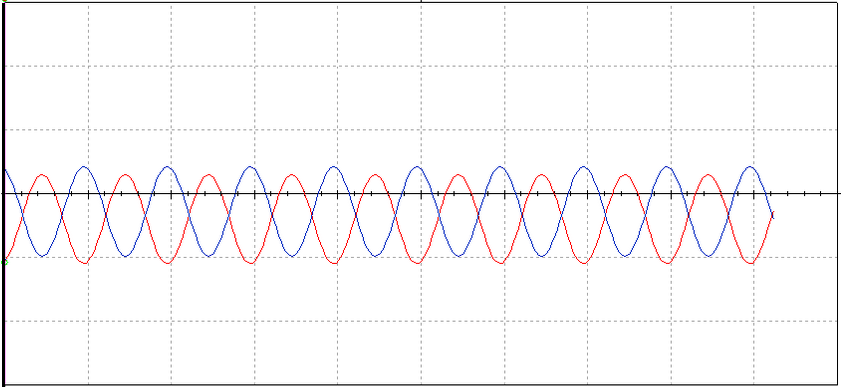
2. Connect the input terminal of the op-amp (terminal 2 for inverting amplifier and terminal 3 for non-inverting amplifier) to function generator and output terminal (pin number 6) to virtual CRO.

3. Apply +15 V at pin 7 and -15 V at pin 4.

4. Give the input from function generator and observe the output on virtual CRO. Note down the peak voltages of input and output and calculate the voltage gain.

Expected Wave form:

Inverting Amplifier



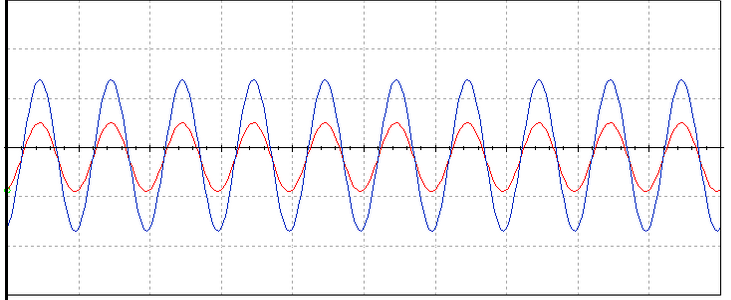
Note: Red is input and Blue is output.

Tabulation:

|  |  |  |
| --- | --- | --- |
| S. no. | Gain | V0 = Vi(-Rf/Rin) |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

Expected Wave form:

Non Inverting Amplifier



Note: Red is input and Blue is output.

Tabulation:

|  |  |  |
| --- | --- | --- |
| S. no. | Gain | V0 = Vi(1+Rf/Rin) |
|  |  |  |
|  |  |  |
|  |  |  |

**Conclusions:**

**Experiment 7**

**Study of Integrator** **and differentiator circuits using IC 741 Op-Amp**

**AIM**: To study the working of Op-amp as integrator and differentiator.

**Apparatus:** NI ELVIS II+

Connecting probes

Resistors (100K, 10k)

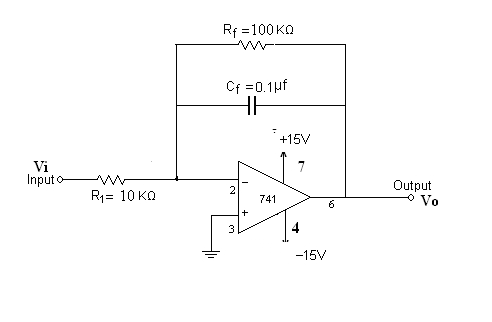
Diode (IN4001)

Op-Amp (741)

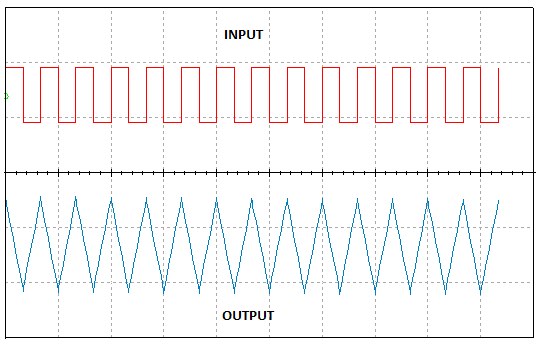
Capacitor (0.1 µF)

**CIRCUIT DIAGRAM**:

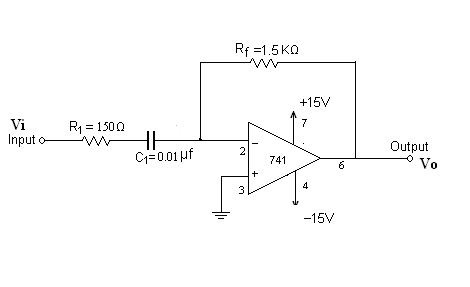
Integrator



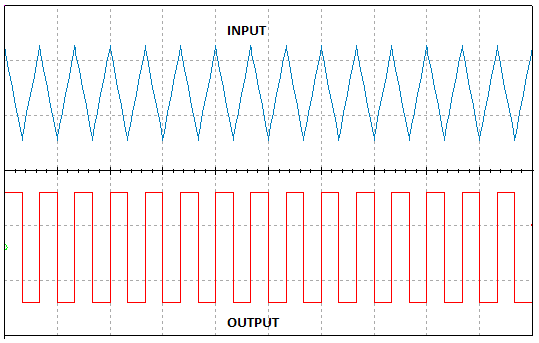
**OUTPUT WAVEFORM:**

****

**DIFFERENTIATOR CIRCUIT:**

****

**OUTPUT WAVEFORM:**

****

Procedure:

1. Connect the circuit as shown in fig.
2. Apply a symmetrical square wave of 2Vp-p amplitude and 1KHZ frequency.
3. Connect the input and output of the circuit to channel 0 and channel 1 of the CRO respectively and observe the waveforms.
4. Draw the waveforms along with the level on a graph.
5. Compare the practical values with theoretical values.
6. Repeat the same for sine-wave.

**Conclusions:**

**Experiment 8**

**Design of Oscillator Circuit using 555 timer**

Aim: To Study and design of oscillator circuit using 555 timers.

**Apparatus:**

NI ELVIS II+

Resistors (2.2 K)

Capacitors

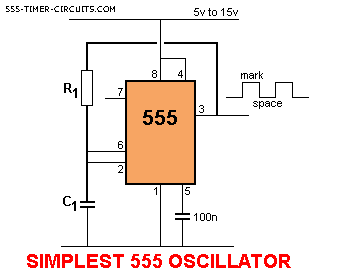
IC 555 Timer

Virtual oscilloscope

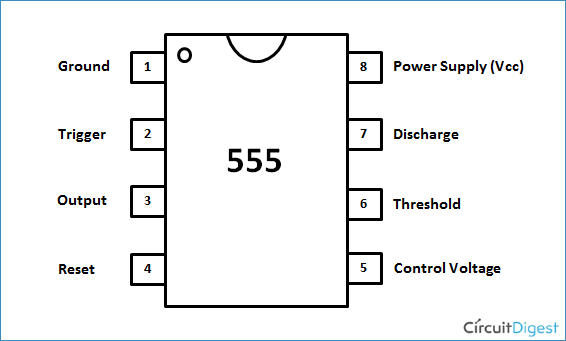
Virtual DC Power Supply

Connecting wires

**Circuit Diagram:**



**IC Pin Configuration:**

****

**Procedure:**

1. Connect the circuit as given in the figure above on NI ELVIS board.

2. Apply +15 V at pin 8

3. Observe the output waveform at pin 3 by using virtual CRO

4. Note down the output voltage peak voltage.

**Conclusions:**

**Experiment 9**

**STUDY OF FREQUENCY RESPONSE of LOW PASS AND HIGH PASS RC FILTERS**

Aim: 1. To analyse the effect of varying frequency to the output voltage of low-pass and high-pass filter

2. To plot the output voltage-frequency response of RC low-pass and high-pass filter.

**Apparatus:**

NI ELVIS II +

Resistors (10 ΩK)

Capacitor (0.01 µF)

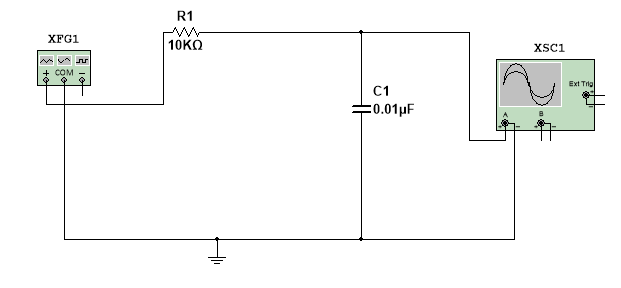
Connecting probes

Multisim (virtual function generator, virtual CRO)

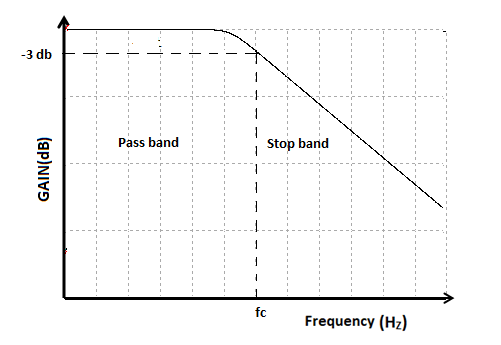
Connecting wires

**CIRCUIT DIAGRAM**:

**LOW PASS FILTER:**

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**Expected Wave Form:**

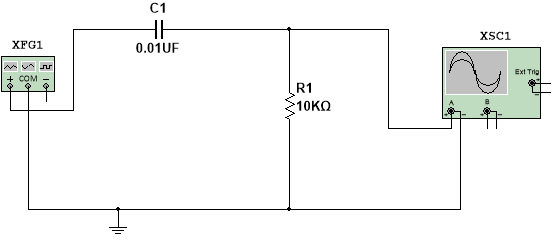


**Calculations:**

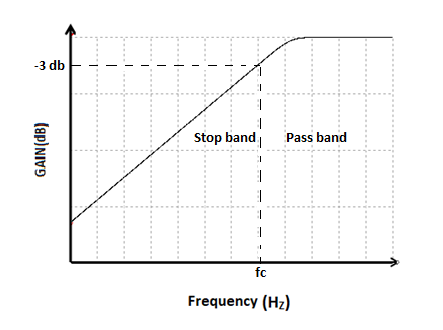
**Table 1:**

|  |  |  |
| --- | --- | --- |
| Frequency (Hz) | 20 log (Vout/Vin) | Phase |
| 1 |  |  |
| 10 |  |  |
| 100 |  |  |
| 1000 |  |  |
| 10000 |  |  |
| 100000 |  |  |
| 1000000 |  |  |

**HIGH PASS FILTER:**

****

**Magnitude Wave Form:**

****

**Calculations:**

**Table 2:**

|  |  |  |
| --- | --- | --- |
| Frequency (Hz) | 20 log (Vout/Vin) | Phase |
| 1 |  |  |
| 10 |  |  |
| 100 |  |  |
| 1000 |  |  |
| 10000 |  |  |
| 100000 |  |  |
| 1000000 |  |  |

**PROCEDURE:**

***Low-pass Filter***

1. Construct the Lowpass filter circuit as shown above
2. Set Vin to 10 Vpp sine wave in function generator at 1000 Hz.
3. Observe the input at CH 0 and output at CH 1.
4. Record CH 1 peak to peak value, which is output voltage, Vout of the circuit in table 1.
5. Increase the frequency as stated in table 1. Record the CH 2 peak to peak value each time the frequency increased in table 1. Make sure that Vin is maintaining at 10Vpp each time you increased the frequency.
6. Based on your result in table 1, plot the gain versus Frequency in the semi-log graph paper provided.
7. Calculate the cut-off frequency, fc according to the values for R and C as shown in the figures.
8. From the graph, find the cut-off frequency by tracing the frequency where the magnitude of the output voltage is -3db (70.7 % of from the maximum value).

***High-pass Filter***

1. Construct the high pass filter circuit as show in the figure. Connect the function generator and oscilloscope as shown in the figure.
2. Set Vin to 10Vpp at 100Hz sine wave.
3. Repeat steps from (c) given above. Write the values in table 2.

**Conclusions:**

**Experiment 10**

**DESIGN OF BASIC LOGIC GATES**

AIM: To study and verify truth table of logic gates.

**Apparatus:**

NI ELVIS II+

Connecting probes

Resistors (1K)

Diode (IN4001)

Transistor (2N3904)

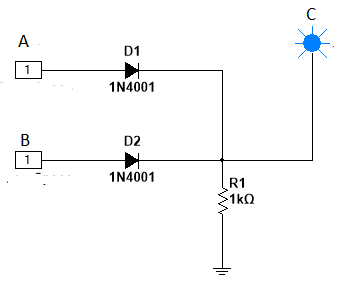
Virtual DC Power Supply

Connecting wires

**CIRCUIT DIAGRAM**:

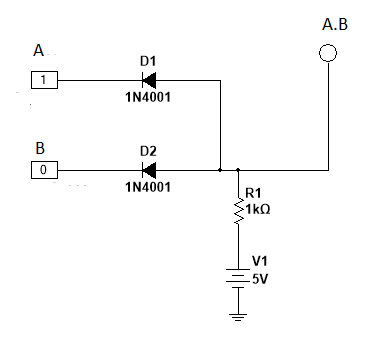
**OR GATE TRUTH TABLE**

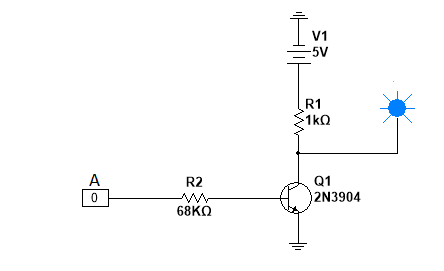
|  |  |  |
| --- | --- | --- |
| A | B | A+B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



**AND GATE TRUTH TABLE**

|  |  |  |
| --- | --- | --- |
| A | B | A\*B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

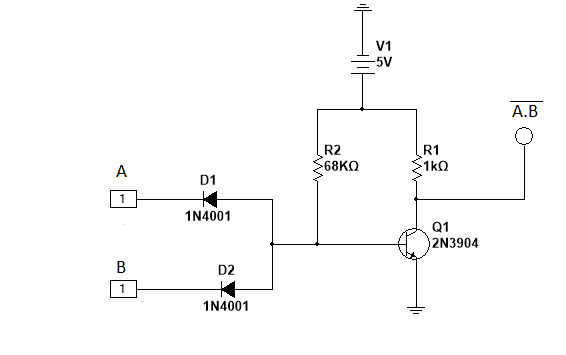


**NOT GATE: TRUTH TABLE**

|  |  |
| --- | --- |
| A |  |
| 0 | 1 |
| 1 | 0 |

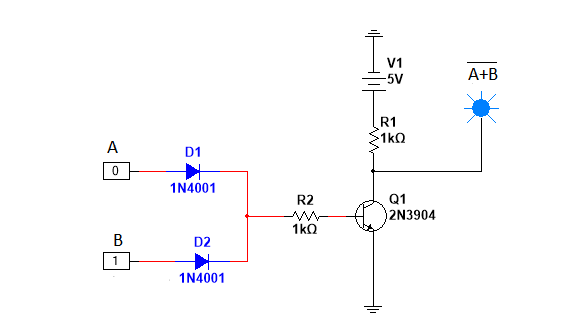
**NAND GATE: TRUTH TABLE**

|  |  |  |
| --- | --- | --- |
| A | B |  |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



**NOR GATE: TRUTH TABLE**

|  |  |  |
| --- | --- | --- |
| A | B |  |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



Procedure:

1. Connect the circuits diagram on the NI ELVIS II+ bread board using the components and connecting wires as per the circuit diagram.
2. Give the 5 V supply from bread board to the circuit as shown.
3. Verify the truth table using digital writer and digital reader.
4. Repeat the first three steps for the remaining gates and verify the truth tables.

Conclusion: